IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Douglas J. Cutter et al.	§	Group Art Unit: Unassigned
Prior Application Serial No.: 08/813,525	§	
Prior Application Filed: March 7, 1997	§	
	§	Examiner: Unassigned
Serial No.: Unassigned	§	
Filed: Herewith	§	
	§	Atty. Docket: MCRO:181--1/FLE
For: METHOD AND APPARATUS FOR CHECKING THE RESISTANCE OF PROGRAMMABLE ELEMENTS	§	95-0580.01

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Pursuant to 37 C.F.R. § 1.10, I hereby certify that I am personally depositing this paper or fee with the U.S. Postal Service, "Express Mail Post Office to Addressee" service on the date indicated above in a sealed envelope (a) having the above-numbered Express Mail label and sufficient postage affixed, and (b) addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

February 5, 2001 — *Date*

Cynthia L. Hayden — *Cynthia L. Hayden*

Assistant Commisioner
For Patents
Washington, D.C. 20231

Dear Sir:

PRELIMINARY AMENDMENT

Prior to examination of the above-referenced application, please amend the application as follows:

IN THE SPECIFICATION

Insert before the first line the sentence: --This application is a Continuation of application Serial No. 08/813,525, filed March 7, 1997.--

Page 10, line 19, change "node 5" to -- node 55 --.

Page 12, line 21, change "DVC2" to -- DVC2! --.

Page 13, line 1, change "circuit 20" to -- circuit 19 --.

Page 13, line 2, change "comparator 20" to -- comparator circuit 19 --.

Page 13, line 5, change "circuit 20" to -- circuit 19 --.

Page 13, line 10, change "circuit 20" to -- circuit 19 --.

IN THE DRAWINGS

In Fig. 6, delete reference numeral "20" and substitute reference numeral -- 19 -- therefor.

IN THE CLAIMS

Please cancel claims 2-27 without prejudice.

Please add new claims 28-48 as set forth below:

28 (new). A method of determining whether a programmable element in an integrated circuit has been programmed, comprising the acts of:

producing a first voltage at a first node based on a resistance of the programmable element;

producing a second voltage at a second node based on a known resistance; and

comparing the first and second voltages and producing an output signal having a binary value in response to the comparison, the binary value of the output signal indicating whether the programmable element has been programmed.

29 (new). The method of claim 28, comprising the acts of:

equilibrating the voltages at the first and second nodes; and

performing the act of comparing the first and second voltages after sufficient time has elapsed to allow the first and second voltages to change, respectively, based on the known resistance and the resistance of the programmable element.

30 (new). The method of claim 29, wherein the voltages at the first and second nodes are equilibrated at the same approximate voltage between V_{CC} and zero volts.

31 (new). A method of determining whether a programmable element in an integrated circuit has been programmed, the method comprising the acts of:

providing a first node at which a first voltage is produced based on a resistance of the programmable element;

providing a second node at which a second voltage is produced based on a known resistance;

equilibrating the voltages at the first and second nodes; and

comparing the voltages at the first and second nodes and producing an output signal having a binary value in response to the comparison, the binary value of the output signal indicating whether the programmable element has been programmed.

32 (new). An apparatus for determining whether a programmable element in an integrated circuit has been programmed, the apparatus comprising:

a programmable circuit comprising:

a programmable element having a resistance; and

a first node at which a voltage may be developed that is based on the resistance of the programmable element;

a reference generator adapted to produce a reference voltage at a second node, the reference voltage being based on the value of a known resistance; and

a comparison circuit adapted to compare the voltage on the first node to the reference voltage on the second node and produce an output signal having a binary value indicative of whether the programmable element has been programmed.

33 (new). The apparatus of claim 32, comprising an equilibrating circuit adapted to equilibrate the voltages at the first and second nodes.

34 (new). The apparatus of claim 32, wherein the programmable element comprises an antifuse element.

35 (new). The apparatus of claim 32, wherein the programmable element comprises an ovonic element.

36 (new). In an integrated circuit, an apparatus comprising:

a plurality of programmable circuits, each programmable circuit comprising:

a programmable element having a resistance; and

a first node at which a voltage may be developed that is based on the resistance of the programmable element,

wherein the first nodes of all the plurality of programmable circuits being joined in a common connection;

selection circuitry adapted to select one of the plurality of programmable circuits;

a reference generator adapted to produce a reference voltage at a second node, the reference voltage being based on the value of a known resistance; and

a comparison circuit adapted to compare the voltage at the first node of the selected programmable circuit to the reference voltage at the second node and to produce an output signal having a binary value indicative of whether the programmable element has been programmed.

37 (new). The apparatus of claim 36, comprising an equilibrating circuitry adapted to equilibrate the voltages at the first and second nodes.

38 (new). The apparatus of claim 36, comprising circuitry adapted to vary the value of the known resistance.

39 (new). The apparatus of claim 36, wherein the comparison circuit comprises a comparator.

40 (new). The apparatus of claim 36, wherein the programmable element comprises an antifuse element.

41 (new). The apparatus of claim 36, wherein the programmable element comprises an ovonic element.

42 (new). An integrated circuit, comprising:

a plurality of programmable circuits, each programmable circuit comprising:

a programmable element having a resistance; and

a first node at which a voltage may be developed that is based on the resistance of the programmable element,

wherein the first nodes of all programmable circuits being joined in a common connection;

a decoder adapted to decode a first address signal and to send a first enabling signal to each of the plurality of programmable circuits;

a reference circuit adapted to produce a reference voltage at a second node, the reference voltage being based on the value of a known resistance; and

a comparator circuit adapted to compare the voltage at the first node of the selected programmable circuit to the reference voltage at the second node and to produce an output signal having a binary value indicative of whether the programmable element has been programmed.

43 (new). The apparatus of claim 42, wherein the the programmable element comprises an antifuse element.

44 (new). The apparatus of claim 42, wherein the programmable element comprises an ovonic element.

45 (new). A semiconductor memory device, comprising:

a memory array;

a plurality of programmable circuits, each programmable circuit comprising:

a programmable element having a resistance; and

a first node at which a voltage may be developed that is based on the resistance of the programmable element,

wherein the first nodes of all programmable circuits being joined in a common connection;

a circuit adapted to produce a first voltage at a first node based on a known resistance;

a reference circuit adapted to produce a second voltage at a second node based on the resistance of a programmable element; and

a comparison circuit adapted to compare the first voltage to the second voltage and producing an output signal having a binary value in response to the comparison, the binary value of the output signal indicating whether the programmable element has been programmed.

46 (new). The apparatus of claim 45, comprising:

an equilibrating circuit adapted to equilibrate the voltages at the first and second nodes.

47 (new). The apparatus of claim 45, wherein the programmable element comprises an antifuse element.

48 (new). The apparatus of claim 45, wherein the programmable element comprises an ovonic element.

REMARKS

Claims 2-27 have been canceled without prejudice. New claims 28-48 have been added. Consideration of the application as amended is respectfully requested.

If the Examiner believes that a telephonic interview will help speed this application toward issuance, Applicants invite the Examiner to contact the undersigned at (281) 970-4545.

General Authorization for Extensions of Time

In accordance with 37 C.F.R. § 1.136, Applicants hereby provide a general authorization to treat this and any future reply requiring an extension of time as incorporating a request therefor. Furthermore, Applicants authorize the Commissioner to charge the appropriate fee for any extension of time to Deposit Account No. 13-3092; Order No. MCRO:181--1/FLE (95-0580.01).

Respectfully submitted,

Date: February 5, 2001

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